REMARKS/ARGUMENTS

Applicants have received the Office action dated July 15, 2004, in which the Examiner objected to claim 14 and rejected claims 1-27 under 35 U.S.C. § 102(e). In this Response, Applicants cancel claims 6-9, 15-18 and 25, and amend claims 1, 10, 14, 19, 24 and 26. Based on the arguments and amendments contained herein, Applicants respectfully submit that all remaining pending claims are in condition for allowance.

I. THE § 102 CLAIM REJECTIONS

With regard to claims 1, 10, and 19, the Examiner rejected the claims as anticipated by Merchant (U.S. Pat. No. 6,665,792). Merchant discloses a memory ordering buffer (MOB) that "includes a load buffer 141 for recording all load operations and a store buffer 143 for recording all store operations." Col. 6, lines 8-10. When a load is processed, the MOB provides the information necessary to determine "whether or not this load must be replayed. [sic] by examining all entries in store buffer 143A to determine if there is at least one store instruction in the store buffer 143A that is older than this load instruction and has its invalid store flag 510 set." Col. 14, lines 1-5. Thus, Merchant requires that the entire store buffer be searched each and every time a load executes in order to identify a load/store order violation.

The Examiner stated that "Merchant has taught a computer system, comprising...[a] microprocessor...[w]herein said microprocessor...[c]reates a store set for the load...adds the store to the store set...[and] [r]e-processes said load if said poison value associated with said store indicates the store has been poisoned." The Examiner further indicated that "a 'store set' corresponding to entries in the load buffer [the load buffer 141 of the MOB], the store buffer [the store buffer 143 of the MOB] and the bus queue is created upon detecting of a load/store order violation by making entries for the corresponding load and store instructions in their respective buffers."

As amended, claim 10 is directed to "a computer system comprising: a microprocessor comprising a store set identifier table...wherein said microprocessor...creates a store set comprising a store set identifier value that

identifies the store of the load/store order violation, and wherein the store set identifier links the load to the store...saves the store set to the store set identifier table...re-processes said load if said poison value associated with said store indicates through the store set dependence that the store has been poisoned...and applies said poison value through the store set dependence to subsequent load/store order violation occurrences." Merchant does not teach or even suggest a system comprising a microprocessor that creates and saves a "store set," in particular a store set that comprises a store set identifier value that identifies the store and that links the load to the store. Merchant also does not teach or suggest a system with a microprocessor that reprocesses the load based on a poison value that indicates through the store set that the store set is poisoned, or that reapplies the poison value through the store set to subsequent load/store order violation occurrences. At least for these reasons, claim 10 and dependent claims 11-14 are allowable over Merchant.

Similarly, as amended claim 1 is directed to a method of processing instructions in a microprocessor comprising, among other actions, creating a store set comprising creating a store set comprising a store set identifier that identifies the store of the load/store order violation, and wherein the store set identifier associates the load with the store and saving the store set to a store set identifier table. Claim 1 as amended further comprises setting a setting a poison value that indicates through a store set dependence that that the store is poisoned, re-processing said load if said poison value associated with said store indicates through the store set dependence that the store has been poisoned, and applying said poison value through the store set dependence to subsequent load/store order violation occurrences. Merchant does not teach or suggest a method comprising the limitations described, and at least for these reasons claim 1 and dependent claims 2-5 are allowable over Merchant.

Likewise, claim 19 is directed to a microprocessor that comprises a store set identifier table, wherein the store set comprises a store set identifier value that identifies a store of a load/store violation, as well as logic that creates a store set linked to the load. The logic described in claim 19 also saves the store

set to the store set identifier table, and if the store is poisoned, sets a poison value that indicates through a store set dependence that the store is poisoned. Further, the logic of claim 19 re-processes said load if said poison value associated with said store indicates through the store set dependence the store has been poisoned, and reapplies said poison value through the store set dependence to subsequent load/store order violation occurrences. Merchant does not teach or suggest a microprocessor comprising the limitations described, and at least for these reasons claim 19 and dependent claims 20-23 are allowable over Merchant.

With regard to claim 24, the Examiner rejected the claim as anticipated by Merchant (U.S. Pat. No. 6,665,792). Merchant teaches an embodiment wherein "if an invalid store flag 510 is set for one or more store instructions in the store buffer 143A, this will cause all logically subsequent (or programmatically younger) load instructions to be replayed... ." Taking claim 15 as exemplary, the Examiner stated that "Merchant has taught a computer system comprising...[a] microprocessor...[w]herein said microprocessor...[i]f said data is stale sets a value associated with said store...[and] if said value is set, reprocesses said load to execute after said data is no longer stale."

As amended, claim 24 is directed to a microprocessor comprising a store set identifier table that comprises a store set associated with said load, wherein said store set comprises a store set identifier that identifies said store of a load/store violation. The microprocessor of claim 24 also comprises logic that establishes said store set for said load to include said store, and saves said value associated with said store in said store set identifier table. Merchant does not teach or suggest a microprocessor comprising the limitations described, and at least for these reasons claim 24 and dependent claims 26-27 are allowable over Merchant.

Additionally, in amending claim 24 as described, the limitations of claim 25 were incorporated into claim 24, and for this reason Applicants cancel claim 25. Also, claim 26 was amended to reflect the cancellation of claim 25 and the amendments to claim 24.

II. THE CLAIM OBJECTION

The Examiner objected to claim 14 as lacking antecedent basis in the claims for the limitation "The method of claim 13." Applicants have corrected claim 14 to read "The system of claim 13" as requested by the Examiner.

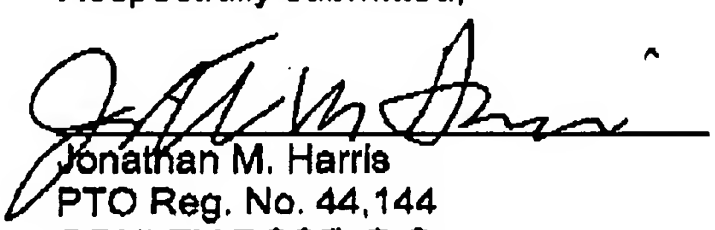
III. CONCLUSION

Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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